SPECIFICATIONS

PXIe-5745

12-Bit, 6.4 GS/s, 2-Channel PXI FlexRIO Signal Generator

This document lists the specifications for the PXIe-5745. Specifications are subject to change without notice. For the most recent device specifications, refer to *ni.com/support*.

Contents

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

NATIONAL INSTRUMENTS

Specifications are *Typical* unless otherwise noted.

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <0..3>[1]	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>[1]	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

Table 2. Digital I/O Single-Ended DC Signal Characteristics[2]

Voltage Family	V_{IL}	V_{IH}	V_{OL} (100µA load)	V_{OH} (100µA load)	Maximum DC Drive Strength
3.3 V	0.8 V	2.0 V	0.2 V	3.0 V	24 mA
2.5 V	0.7 V	1.6 V	0.2 V	2.2 V	18 mA

[1] Multi-gigabit transceiver (MGT) signals are available on devices with KU040 and KU060 FPGAs only.

[2] Voltage levels are guaranteed by design through the digital buffer specifications.

Table 2. Digital I/O Single-Ended DC Signal Characteristics[2] (Continued)

Voltage Family	V_{IL}	V_{IH}	V_{OL} (100µA load)	V_{OH} (100µA load)	Maximum DC Drive Strength
1.8 V	0.62 V	1.29 V	0.2 V	1.5 V	16 mA
1.5 V	0.51 V	1.07 V	0.2 V	1.2 V	12 mA
1.2 V	0.42 V	0.87 V	0.2 V	0.9 V	6 mA

Digital I/O High-Speed Serial MGT[3]

Note MGTs are available on devices with KU040 and KU060 FPGAs only.

Data rate	500 Mbps to 16.375 Gbps, nominal
Number of Tx channels	4
Number of Rx channels	4
I/O AC coupling capacitor	100 nF

Reconfigurable FPGA

PXIe-5745 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PXIe-5745 FPGA options.

Table 3. Reconfigurable FPGA Options

	KU035	KU040	KU060
LUTs	203,128	242,200	331,680
DSP48 slices (25 × 18 multiplier)	1,700	1,920	2,760
Embedded Block RAM	19.0 Mb	21.1 Mb	38.0 Mb
Data Clock Domain	200 MHz, 16 samples per cycle per channel (dual channel mode), 32 samples per cycle (single channel mode)		
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)		

[2] Voltage levels are guaranteed by design through the digital buffer specifications.
[3] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Table 3. Reconfigurable FPGA Options (Continued)

	KU035	KU040	KU060
Data transfers	DMA, interrupts, programmed I/O	DMA, interrupts, programmed I/O, multi-gigabit transceivers	
Number of DMA channels	60		

Note The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Analog Output

General Characteristics

Number of channels	2, single-ended, simultaneously updated
Connector type	SMA
Output impedance	50 Ω
Output coupling	AC

Update rate	
Internal Sample Clock, 2x interpolation	6.4 GS/s
External Sample Clock, 2x interpolation	6.4 GS/s[4]
Data rate (per channel)	
Dual channel mode	3.2 GS/s, real
Single channel mode	3.2 GS/s, complex
Digital-to-analog converter (DAC)	DAC38RF82, 12-bit resolution
Output latency[5]	
DUC disabled	211 ns
DUC enabled	221 ns

Typical Specifications

Note Due to a silicon flaw in the TI DAC38RF82 chip, there is a 0.5% chance of seeing a 50 mV glitch at the output of either channel after a bitfile re-download, invoking the Reset method explicitly or by closing the FPGA reference, or committing a new configuration.

Full-scale output power[6]	
Dual Channel Mode	2.85 dBm (878 mVpp)
Single Channel Mode	-3.33 dBm (431 mVpp)
Bandwidth (-3 dB)[7]	
Dual Channel Mode	3 MHz to 1.53 GHz
Single Channel Mode (no anti-image filter)	60 MHz to 2.85 GHz
Single Channel Mode (with anti-image filter)	60 MHz to 2.35 GHz

[4] To achieve this update rate when using an external sample clock, inject a 3.2 GS/s clock into the REF/CLK IN port and enable 2x interpolation.

[5] LabVIEW diagram to SMA output

[6] Into a 50 Ω load.

[7] Normalized to 10 MHz in dual channel mode and 200 MHz in single channel mode. 2x interpolation and inverse sinc filter enabled.

Table 4. Single Tone Spectral Performance, Dual Channel Mode[8]

	Generation Frequency	
	501 MHz	**1.01 GHz**
2nd HD (dBc)	-67.8	-61.7
3rd HD (dBc)	-63.0	-62.0
SFDR (dBc)	-63.0	-61.7

Table 5. Single Tone Spectral Performance, Single Channel Mode[8]

	Generation Frequency
	1.01 GHz
2nd HD (dBc)	-62.4
3rd HD (dBc)	-67.3
SFDR (dBc)	-62.4

Table 6. IMD3 Performance, Dual Channel Mode, Measured[9]

	Generation Frequency	
	501 MHz and 511 MHz	**1.005 GHz and 1.015 GHz**
IMD3 (dBc)	-73.9	-67.6

Table 7. Noise Spectral Density[10]

	501 MHz Generation Frequency		
Mode	$\frac{nV}{\sqrt{Hz}}$	$\frac{dBm}{Hz}$	$\frac{dBFS}{Hz}$
Dual Channel	1.18	-165.5	-168.4
Single Channel	0.941	-167.5	-164.2

[8] DC, 3.2 GHz, output corrected to 0 dBFS by inverse sinc filter, 2x interpolation, no anti-image filter.

[9] 2x interpolation, inverse sinc filter enabled, each tone corrected to -6 dBFS by inverse sinc filter.

[10] Measured > 50 MHz offset from fundamental. 2x interpolation and inverse sinc filter enabled. Noise spectral density value depends on output tone frequency. See DAC38RF82 datasheet for noise spectral density results at other tone frequencies.

Figure 1. Single Tone Spectrum (Dual Channel Mode, 501 MHz 0 dBFS), Measured[11]

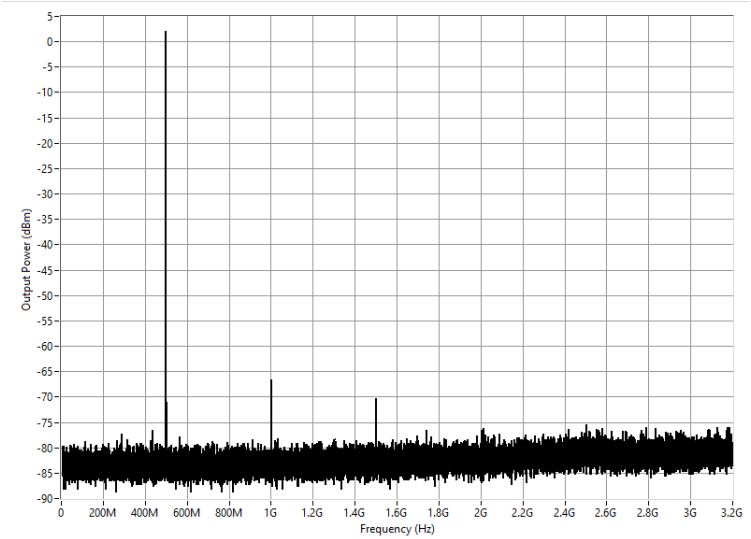
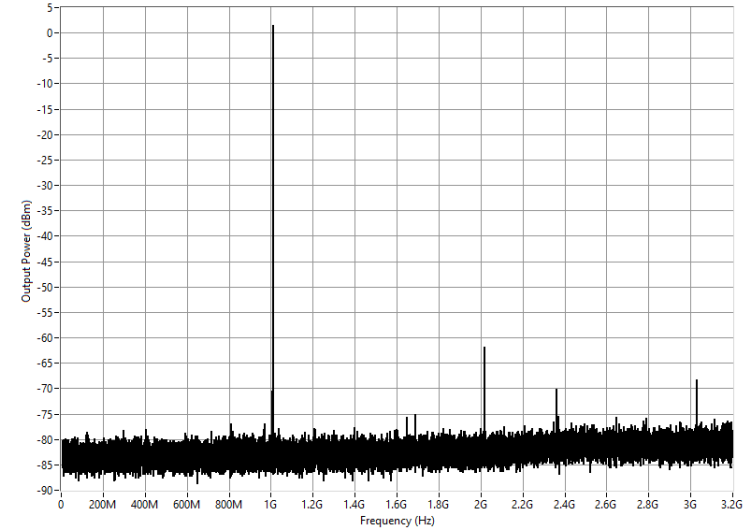
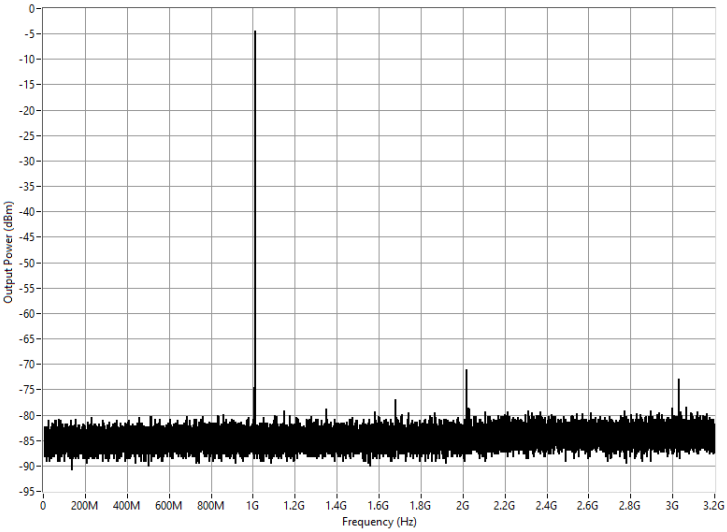


Figure 2. Single Tone Spectrum (Dual Channel Mode, 1.01 GHz 0 dBFS), Measured[11]



[11] 2x interpolation. Output corrected to 0 dBFS by inverse sinc filter. 10 kHz resolution bandwidth.

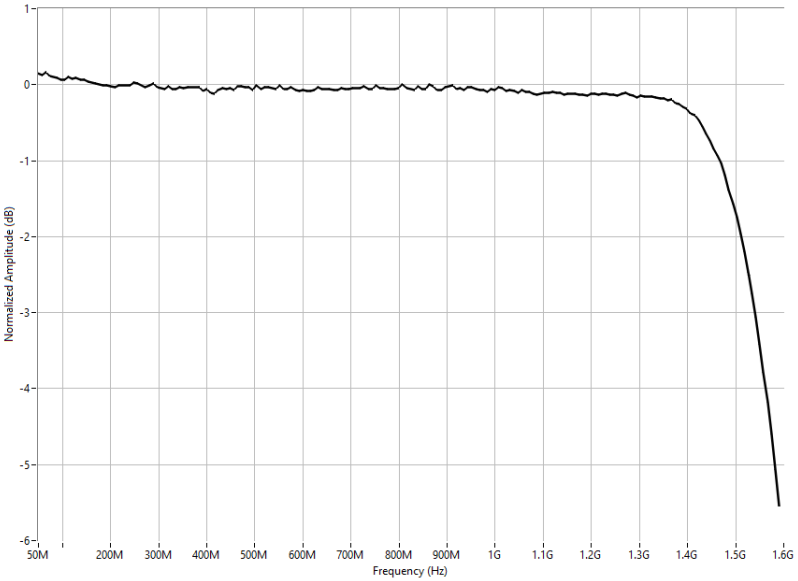
Figure 3. Single Tone Spectrum (Single Channel Mode, 1.01 GHz 0 dBFS), Measured[11]



Channel-to-channel crosstalk, measured[12]	
100 MHz	-82 dBc
500 MHz	-91 dBc
1.0 GHz	-90 dBc
1.5 GHz	-88 dBc
2.0 GHz	-82 dBc
2.5 GHz	-82 dBc

[12] Aggressor channel generating a full-scale output into a 50 ohm terminator

Figure 4. Analog Output Dual Channel Mode Frequency Response, Measured [13]



[13] -6 dBFS, 2x Interpolation, inverse sinc filter enabled, no anti-image filter, normalized to 200 MHz.

Figure 5. Analog Output Single Channel Mode Frequency Response, No Anti-Image Filter, Measured[13]

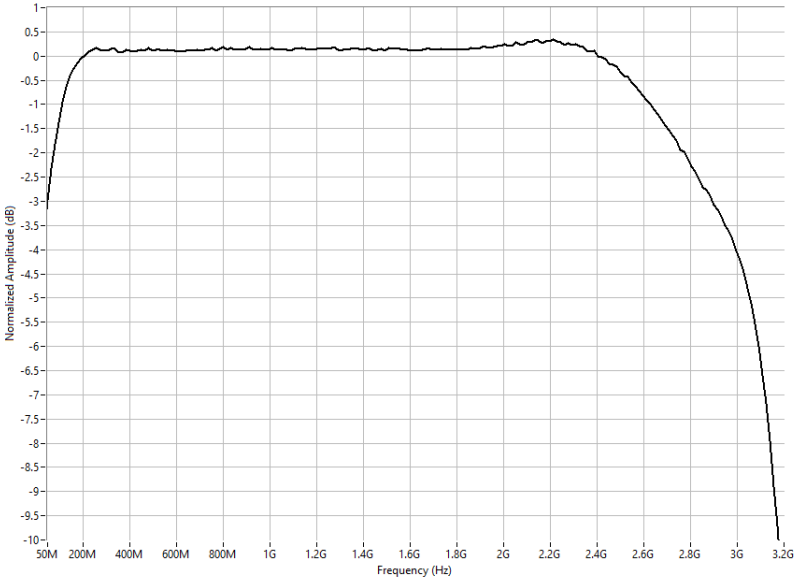
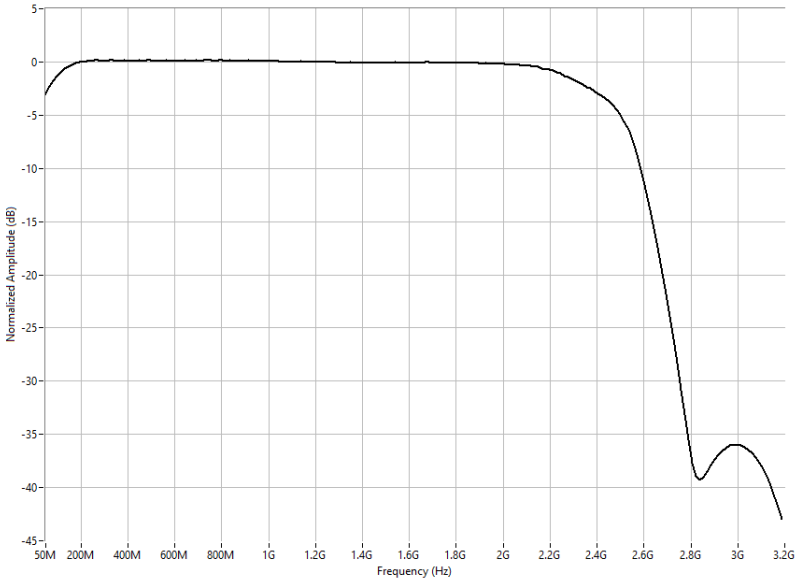
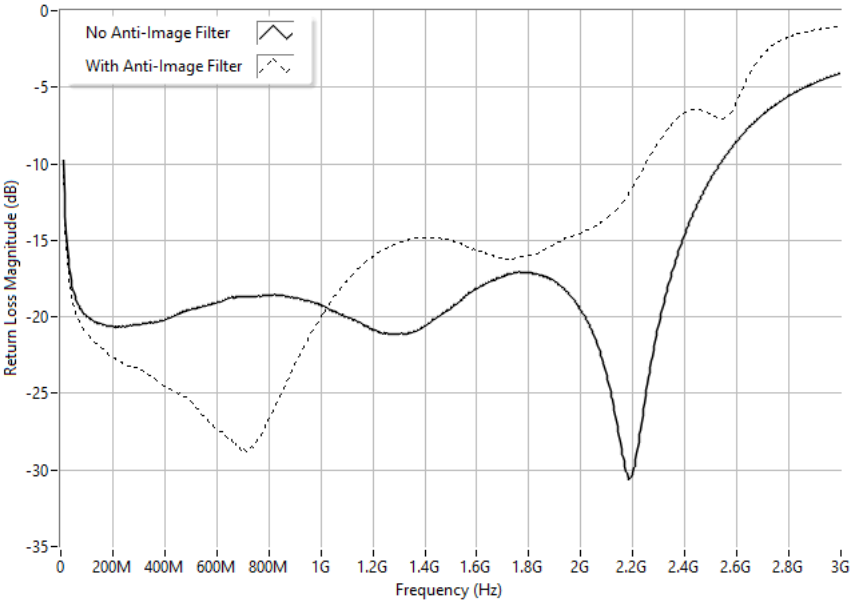


Figure 6. Analog Output Single Channel Mode Frequency Response With Anti-Image Filter, Measured[14]



[14] -6 dBFS, 2x Interpolation, inverse sinc filter enabled, normalized to 200 MHz.

Figure 7. Analog Output Return Loss, Measured



REF/CLK IN

CLK/REF IN

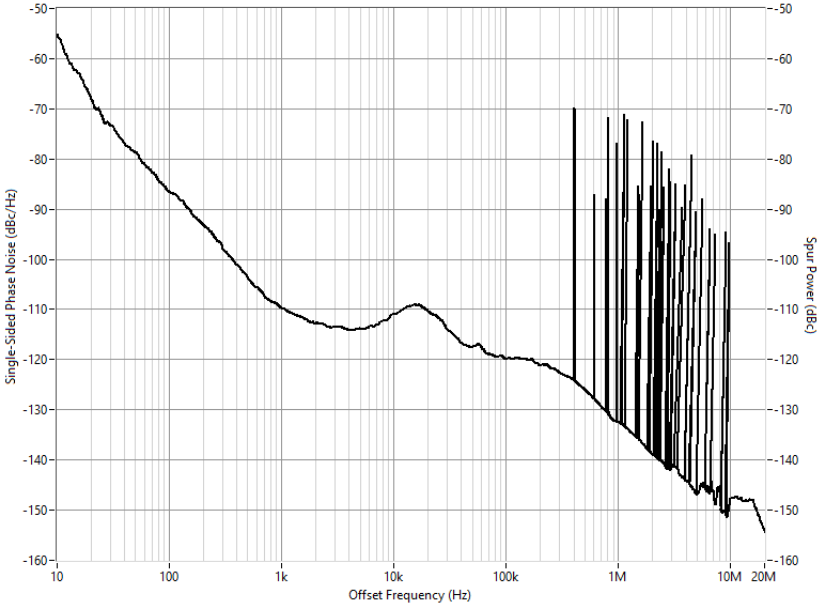
Connector type	SMA
Input impedance	50 Ω
Input coupling	AC
Input voltage range	0.35 V pk-pk to 3.5 V pk-pk, nominal
Absolute maximum voltage	±12 V DC, 4 V pk-pk AC
Duty cycle	45% to 55%
Sample Clock jitter	
Analog output	198.8 fs_{rms}, measured[15]

[15] Integrated from 1 kHz to 30 MHz. Includes the effects of the converter aperture uncertainty, converter PLL circuitry, and the clock circuitry jitter. Excludes trigger jitter.

Table 8. Clock Configuration Options

Clock Configuration	External Clock Frequency	Description
Internal PXI_CLK10[16]	10 MHz	The internal Sample Clock locks to the PXI 10 MHz Reference Clock, which is provided through the backplane.
External Reference Clock (CLK/REF IN)	10 MHz[17]	The internal Sample Clock locks to an external Reference Clock, which is provided through the CLK/REF IN front panel connector.
External Sample Clock (CLK/REF IN)	2.8 GHz to 3.2 GHz	An external Sample Clock can be provided through the CLK/REF IN front panel connector.

Figure 8. Analog Output Phase Noise with 1 GHz Output Tone, Measured



16 Default clock configuration.
17 The external Reference Clock must be accurate to ±25 ppm.

Bus Interface

Form factor	x8 PXI Express, specification v2.1 compliant
Slot compatibility	x4, x8, and x16 PXI Express or PXI Express hybrid slots

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

Physical

Dimensions (not including connectors)	3U, one-slot PXI Express module, 21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)
Weight	490 g (17.3 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[18] (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 4 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

TCLK Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample Clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help* within the *FlexRIO Help*. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

[18] The PXIe-5745 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the *PXI Chassis Manual* for specifications to determine the ambient temperature ranges your chassis can achieve.

Intermodule Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample Clocks of each module.
- All parameters are set to identical values for each module.
- Modules are synchronized without using an external Sample Clock.

Note Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew[19]	80 ps, measured
Skew after manual adjustment	≤10 ps, measured
Sample Clock delay/adjustment	0.4 ps

[19] Caused by clock and analog delay differences. No manual adjustment performed. Tested with a PXIe-1085 chassis with a 24 GB backplane with a maximum slot to slot skew of 100 ps. Measured at 23 °C.